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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,429	04/19/2001	Charles Jay Alpert	AUS920010118US1	3587

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EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,429	ALPERT ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-13 and 17-21* is/are rejected.

7)☒ Claim(s) *6-8, 14-16 and 22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for reconsideration in view of Applicant's arguments and amended claim language.

Response to Arguments

2. Applicant's arguments presented in the 3-14-2005 responses have been fully considered. The Examiner's response is as follows.

2.1 Regarding the Applicant's response to the 35 U.S.C. 112 rejections of claims 5, 13, and 21.

The Examiner thanks the Applicant for amending the claim language and withdraws the earlier 35 U.S.C. 112 rejections of those claims.

2.2 Regarding the Applicant's response to the 35 U.S.C. 101 non-statutory double patenting rejections of claims 1-24.

The Examiner thanks the Applicant's for providing the Terminal Disclaimers and the Examiner withdraws the rejections of claims 1-24 under the Judicially Created Doctrine of obvious type non-statutory double patenting.

2.3 Regarding the Applicant's response to the 35 U.S.C. 102 rejections of Independent **Claims 1, 9 and 17** and dependent **Claims 2, 3, 4, 5, 10, 11, 12, 13, 18, 19, 20 and 21.**

The Examiner notes that the Applicant has amended independent **Claims 1, 9 and 17** and has changed the scope of those claims. In view of Applicant's amended Claim language the Examiner withdraws the 35 U.S.C. 102 rejections of the claims.

2.4 Applicant's arguments with respect to claims 1, 9 and 17 have been considered but are moot in view of the new ground(s) of rejection. An updated search, based on the expanded scope of Applicant's claimed limitations, has revealed new art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Independent **Claims 1, 9 and 17** and dependent **Claims 2, 10 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Varadarajan et al. U.S. Patent 5,838,583** in view of **Alpert et al. U.S. Patent 6,117,182.**

3.1 As regards independent **Claims 1, 9 and 17** the *Varadarajan et al.* reference teaches, *routing* **(Figures 19a, 19b and 19c, Col. 2 Lines 28-43),** *tiles* **(Figure 2 Items 311, 313, Col. 25 Lines 27-58),** *cost calculations* **(Figure 16b item 253, Col. 23 Lines 4-37).**

However, the *Varadarajan et al.* reference does not expressly disclose a minimization algorithm for buffer placement using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one sink.

In the same routing placement art, the Applicant invented a method of optimum buffer placement using an algorithm, the *Alpert et al.* reference discloses, **(Figures 1-7 and Col. 1 lines 15-25, Col. 14 lines 4-11)** and a method for minimization/*optimization* algorithm for buffer placement **(Col. 16 lines 46-52).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the teachings of the *Varadarajan et al.* reference with the teachings of the *Alpert et al.* reference because, both methods disclosed are used to solve the same problem, find the optimal method to place and route circuit elements in a high speed ASIC design **(Alpert et al. SUMMARY of the INVENTION Col. 3 lines 35-67).**

3.2 As regards dependent **Claims 2, 10 and 18** the *Varadarajan et al.* reference teaches *Steiner trees* **(Col. 25 Lines 1-11).**

4. Independent **Claims 1, 9 and 17** and dependent **Claims 2, 3, 4, 10, 11, 12, 18, 19 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nitta et al. Pub. No. US 2001/009031** in view of **Alpert et al. U.S. Patent 6,117,182.**

4.1 As regards Independent **Claims 1, 9 and 7** the *Nitta et al.* reference teaches, *a method for designing buffer and wire placement in an integrated circuit* **(Figure 5, paragraphs 0002 & 0003),** *representing the surface of a integrated circuit as a tile graph* **(Figure 1-4 and paragraphs 0015, 0016, 0017, 0018, 0019, 0020 and 0021** which teach *"blocks"* which are functionally equivalent to *"tiles"*), *receiving an allocation of buffer locations for selected tiles in*

the tile graph (The Examiner notes that it would be inherent that buffers would be placed on an integrated circuit and that the reference discloses routing of *"cells"* **Figure 5 Item 16),** *routing nets between associated sources and sinks "a prohibiting region" is functionally equivalent to a "sink"* **(Figures 12A, 12B, 12C),** *selectively assigning buffer locations within selected tiles* **(Figures 17B, 17A paragraph 0069),** *assign(ing) buffer locations using a cost minimization algorithm* **(Figures 15A & 15B).**

However, the *Nitta et al.* reference does not expressly disclose a minimization algorithm for buffer placement using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one sink.

In the same routing placement art, the Applicant invented a method of optimum buffer placement using an algorithm, the *Alpert et al.* reference discloses, **(Figures 1-7 and Col. 1 lines 15-25, Col. 14 lines 4-11)** and a method for minimization/*optimization* algorithm for buffer placement **(Col. 16 lines 46-52).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the teachings of the *Nitta et al.* reference with the teachings of the *Alpert et al.* reference because, both methods disclosed are used to solve the same problem, find the optimal method to place and route circuit elements in a high speed ASIC design **(Alpert et al. SUMMARY of the INVENTION Col. 3 lines 35-67).**

4.2 As regards dependent **Claims 2, 10 and 18** the *Nitta et al.* reference discloses *Steiner trees* **(paragraph 0010).**

4.3 As regards dependent **Claims 3, 4, 11, 12, 19 and 20** the *Nitta et al.* reference discloses **(paragraph 0030),** which teaches checking wiring capacity through a particular path to avoid path congestion.

5. Independent **Claims 1, 9 and 17** and dependent **Claims 2, 10 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable in view of **"Manhattan or Non-Manhattan? A study of Alternative VLSI Routing Architectures"** by Cheng-Kok Koh and Patrick H, Madden hereafter referred to as the *Koh et al.* reference in view of **Alpert et al. U.S. Patent 6,117,182.**

5.1 As regards independent **Claims 1, 9 and 17** the *Koh et al.* reference teaches, *routing* **(page 47 & page 48),** *tiles* **(page 48),** *cost calculations* **(page 51).**

However, the *Koh et al.* reference does not expressly disclose a minimization algorithm for buffer placement using a single-sink buffer insertion algorithm for one associated sink and a multi-sink insertion algorithm for more than one sink.

In the same routing placement art, the Applicant invented a method of optimum buffer placement using an algorithm, the *Alpert et al.* reference discloses, **(Figures 1-7 and Col. 1 lines 15-25, Col. 14 lines 4-11)** and a method for minimization/*optimization* algorithm for buffer placement **(Col. 16 lines 46-52).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made to have combined the teachings of the *Koh et al.* reference with the teachings of the *Alpert et al.* reference because, both methods disclosed are used to solve the same problem, find the optimal method to place and route circuit elements in a high speed ASIC design **(Alpert et al. SUMMARY of the INVENTION Col. 3 lines 35-67).**

5.2 As regards dependent **Claims 2, 10 and 18** the *Koh et al.* reference teaches *Steiner trees* **(page 48).**

Allowable Subject Matter

6. Dependent **Claims 5-8, 13-16 and 21-24** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The specific formula's disclosed in dependent claims 5, 13 and 21 are neither anticipated nor made obvious by the prior art.

Conclusion

7. **Claims 1-24** have been presented for reconsideration in view of Applicant's arguments and amended claim language. Independent **Claims 1, 9 and 17** and dependent **Claims 2, 3, 4, 5, 10, 11, 12, 13, 18, 19, 20 and 21** have been rejected. Dependent **Claims 5-8, 13-16 and 21-24** have been objected to.

7.1 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Primary Examiner
AU 2123
TC 2100